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Multi-channel tri-gate normally-on/off AlGaN/GaN MOSHEMTs on Si substrate with high breakdown voltage and low ON-resistance

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In this work, we present multi-channel tri-gate AlGaN/GaN metal-oxide-semiconductor high-electron-mobility transistors (MOSHEMTs) for high-voltage applications. A heterostructure with multiple AlGaN/GaN layers was used to form five parallel two-dimensional-electron-gas (2DEG) channels to reduce the ON-resistance (R_{ON}), simultaneously modulated by the 3-dimensional tri-gate electrodes. The tri-gate is a unique technology to control the multi-channels, providing enhanced electrostatics and device performance, and, in turn, the multi-channels are exceptionally suited to address the degradation in drain current ($I_{D,max}$) caused by the tri-gate. With a tri-gate width (w) of 100 nm, normally-on multi-channel tri-gate transistors presented 3×-higher maximum drain current ($I_{D,max}$), 47%-smaller R_{ON}, as well as 79%-higher maximum transconductance ($g_{m,max}$), as compared to counterpart single-channel devices. Using the channel depletion through the tri-gate sidewalls, normally-off operation was also achieved by reducing w below the sidewall depletion width (w_{dep}), resulting in a positive threshold voltage (V_{TH}) of 0.82 V at 1 μA/mm. The devices presented a high breakdown voltage (V_{BR}) of 715 V, which reveals a promising future platform for high-voltage low-R_{ON} GaN transistors. *Published by AIP Publishing.*
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The exceptional properties of GaN heterostructures have led to the development of AlGaN/GaN high electron mobility transistors (HEMTs), demonstrating outstanding potential for high-voltage applications.[1–5] Nevertheless, the performance of current GaN HEMTs is still far below the prospect promised by this material. Further improvements require a significant reduction in R_{ON}, increase in V_{BR}, while maintaining good performance at high switching frequencies.

Among these factors, R_{ON} is intrinsically determined by the electric conductivity of the two-dimensional-electron-gas (2DEG) channel at the AlGaN/GaN interface, given by the product of its sheet carrier concentration (N_s) and mobility (μ). High-Al-content barrier materials have been intensively explored to increase the N_s, which however results in a reduced μ in addition to a more challenging epitaxial growth.[6–9] Moreover, the increased N_s yields a more negative V_{TH} and makes it much more difficult to achieve normally-off operation.

To address these challenges, we present here multi-channel tri-gate metal-oxide-semiconductor high-electron-mobility transistors (MOSHEMTs) [Fig. 1(a)]. This unique architecture offers smaller R_{ON}, due to the large N_s and high μ in the multi-channels,[10–12] and superior gate control with the 3-dimensional tri-gate structure [Fig. 1(b)], integrating multiple parallel transistors in a given footprint for enhanced performance and reduced substrate cost [Fig. 1(c)]. Here, we demonstrate these devices [Fig. 1(d)] using a five-channel AlGaN/GaN-on-Si heterostructure, investigate the impact of tri-gate geometry on the device performance, and present multi-channel tri-gate devices with high breakdown voltage and low R_{ON}.

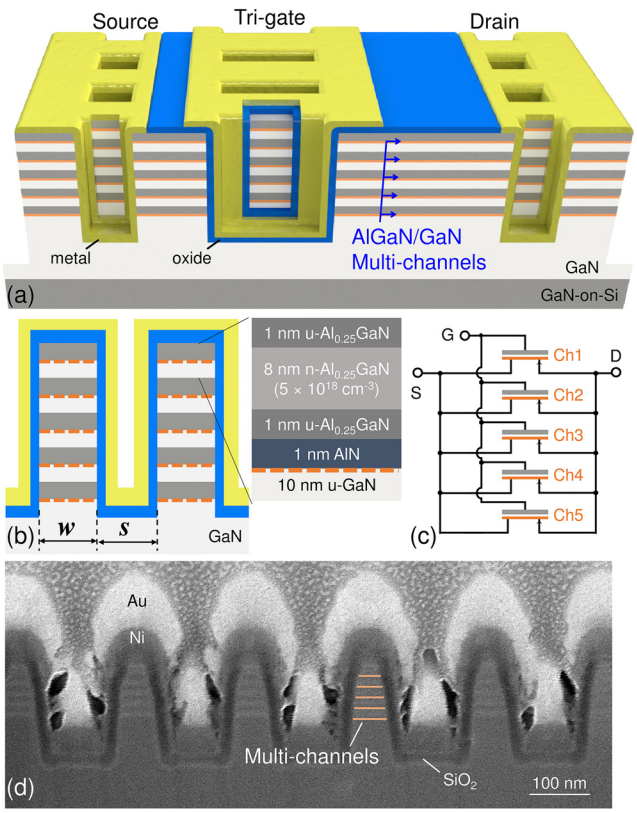

FIG. 1. (a) Schematic of the multi-channel tri-gate AlGaN/GaN MOSHEMT. (b) Cross-sectional schematic of the tri-gate region. The inset shows the heterostructure forming each of the multi-channels. (c) An equivalent circuit of the multi-channel tri-gate MOSHEMT, integrating multiple parallel transistors in a given device footprint for enhanced performance and reduced substrate cost. (d) A cross-sectional SEM image of the tri-gate region, tilted by 52°.

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The multi-channel AlGaN/GaN-on-Si heterostructure in this work consisted of 5 parallel 2DEG channels, formed by a 10 nm-thick AlGaN barrier, a 1 nm-thick AlN spacer, and a 10 nm-thick GaN channel layers. The barrier layer was partially doped with Si at $5 \times 10^{18}\,\mathrm{cm}^{-3}$ [Fig. 1(b)] to enhance the conductivity of multi-channel AlGaN/GaN heterostructures, especially with thin AlGaN barrier layers. Hall measurements revealed a small sheet resistance (R_s) of 230 Ω/sq, N_s of $1.5 \times 10^{13}\,\mathrm{cm}^{-2}$, and μ of $1820\,\mathrm{cm}^2\,\mathrm{V}^{-1}\,\mathrm{s}^{-1}$. A small effective resistivity (ρ_{eff}) of 2.4 mΩ cm was obtained, comparable to other literature results,[13–19] but with a small total thickness (t_{tot}) and higher μ (Fig. 2). Small ρ_{eff} and high μ are crucial to reduce R_{ON}, and a thin t_{tot} facilitates electrostatic gate control and device fabrication (the etching of high-aspect ratio fins and the formation of electrodes around them can be challenging).

The device fabrication started with e-beam lithography to define the fins, which were etched by Ar/Cl_2-based inductively coupled plasma (ICP) with a depth of 200 nm. The fins in the tri-gate region had different w, spacings (s), filling factors (FF), and lengths (l), while the fins in ohmic regions had w and s of 500 nm to contact the multi-channels. Then, an ohmic stack of Ti/Al/Ti/Ni/Au was formed in source and drain regions by e-beam evaporation and a lift-off process, followed by rapid thermal annealing at 800 °C in nitrogen. 25 nm of SiO_2 was deposited by atomic layer deposition (ALD) at 300 °C as the gate dielectric, which was selectively removed by diluted HF (1%) in ohmic regions to expose the source and drain contacts. Finally, the gate was formed using Ni/Au. All current values in this work were normalized by the width of device footprint, unless specified, and the standard deviation was determined from measurements of about 12 devices of each type.

Tri-gates are uniquely suited to control the multi-channels. To illustrate this, we fabricated multi-channel tri-gate transistors with different w but with a long fixed l of 50 μm, which diminished the impact from access and ohmic regions on the extracted device characteristics. Here, the I_D and g_m were normalized by the total width of the long fins, which in this case dominated the device characteristics. More details about these devices can be found in the caption of Fig. 3 as well as Table I. The MOS channels at trenches

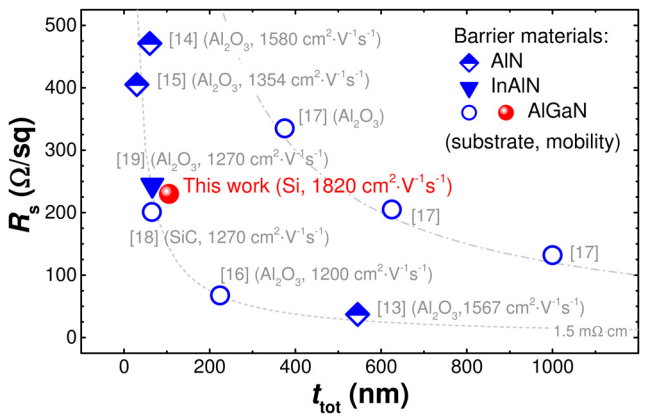

FIG. 2. Comparison of multi-channel structures in this work with literature results. The t_{tot} refers to the total thickness of the multi-channel structure. For a fair comparison, multi-channel structures with unspecified R_s were not included.[20,21]

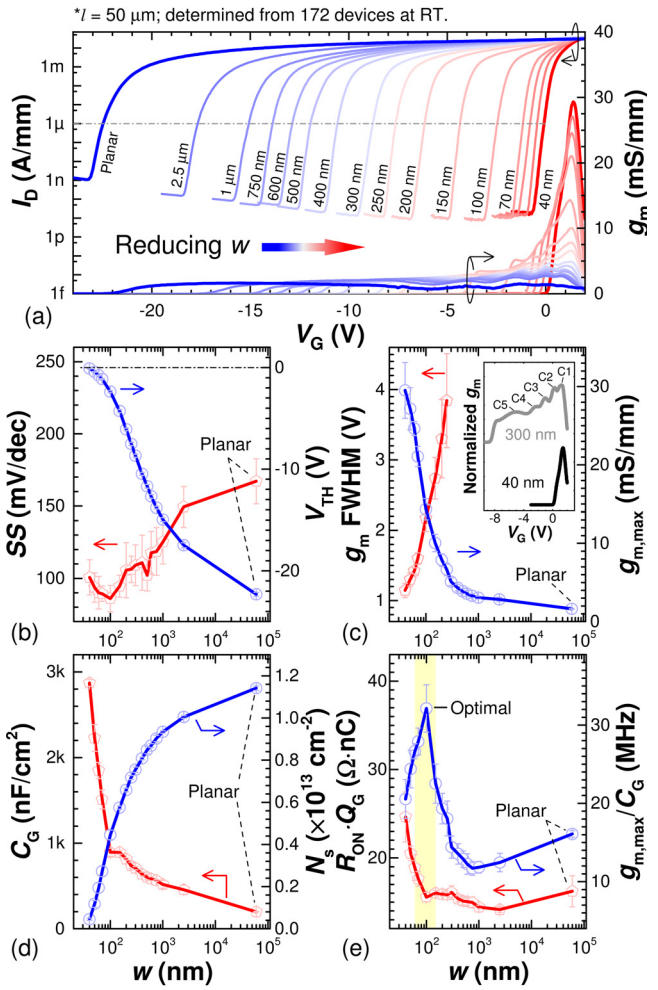

FIG. 3. (a) Transfer characteristics of multi-channel tri-gate MOSHEMTs with different w from 60 μm (planar) to 40 nm, measured at $V_D = 0.5$ V. Width dependence of (b) SS and V_{th} (at 1 μA/mm), (c) $g_{m,max}$ and g_m FWHM, (d) C_G and N_s, and (e) $R_{ON}{\cdot}Q_G$ (Q_G refers to gate charge) and $g_{m,max}/C_G$ values. The inset in (c) shows normalized g_m-V_G plots of devices with w of 40 nm and 300 nm. The R_{ON}, C_G, and Q_G were extracted at $V_G = 2$ V, N_s was extracted at $V_G = 0$ V, and the $g_{m,max}$ was the maximum value of the g_m-V_G characteristics, regardless of the several g_m peaks in transistors with $w > 200$ nm. The C_G and N_s were normalized by the top surface area of the fins. The length of the gate electrode here (L_G) was 51 μm, covering the fins and extending 0.5 μm towards the source and drain. The gate-to-source (L_{GS}) and gate-to-drain (L_{GD}) lengths were 1.5 μm.

were not considered since the measurements were conducted with V_G below the V_{TH} of the MOS channel, which was ~2 V for our oxides and fabrication process,[22] and the conductivity of the MOS channel is much smaller than that of the 2DEG channels.[22]

Figure 3(a) shows the impact of reducing w on the transfer characteristics of the devices. Conventional planar gates are not suited to electrostatically control the multi-channel structure, which is indicated by their large V_{TH} of -22.3 ± 0.2 V (at 1 μA/mm), poor subthreshold swing (SS) of 167 ± 16 mV/dec, and small $g_{m,max}$ of 1.63 ± 0.04 mS/mm. The large $|V_{TH}|$ is caused by the large gate-to-channel distance and the screening effect that shields a lower channel from the gate control unless its upper channel is depleted. The small $g_{m,max}$ and the large SS indicate that control of the multi-channels is not simultaneous. The tri-gate addresses this issue by providing additional electrostatic control from its sidewall portions, which can be

TABLE I. Tri-gate geometry and device characteristics for the 50 μm-long multi-channel tri-gate transistors presented in Fig. 3. The N_s here was normalized by the top surface area of the fins.

w (nm)	s (nm)	FF (%)	l (μm)	Number of fins	Total width of fins (μm)	V_{TH} @ $I_D = 1$ μA/mm (V)	SS @$V_D = 0.5$ V (mV/dec)	$g_{m,max}$ @$V_D = 0.5$ V (μS)	R_{ON} @ $V_G = 2$ V (Ω)	C_G @ $V_G = 2$ V (pF)	Q @ $V_G = 2$ V (pC)	N_s @ $V_G = 0$ V (10^{13} cm^{-2})
40	160	20	50	300	12	-0.08 ± 0.04	101 ± 12	354 ± 43	1212 ± 134	17.2 ± 0.23	20.3 ± 0.6	0.05 ± 0.01
50	150	25	50	300	15	-0.42 ± 0.04	93.7 ± 10	408 ± 40	929 ± 60	16.7 ± 1.2	22.2 ± 1.8	0.12 ± 0.02
60	140	30	50	300	18	-0.78 ± 0.04	90.0 ± 11	443 ± 16	769 ± 47	16.6 ± 0.84	24.6 ± 1.7	0.19 ± 0.02
70	130	35	50	300	21	-1.14 ± 0.05	89.4 ± 5.3	442 ± 27	664 ± 19	15.9 ± 1.1	26.5 ± 1.5	0.27 ± 0.03
100	100	50	50	300	30	-2.37 ± 0.09	86.0 ± 9.2	430 ± 41	487 ± 13	13.4 ± 0.69	32.0 ± 1.3	0.45 ± 0.02
150	150	50	50	200	30	-4.28 ± 0.14	94.5 ± 7.6	301 ± 33	487 ± 8.4	13.4 ± 0.32	32.9 ± 0.7	0.58 ± 0.01
200	200	50	50	150	30	-6.08 ± 0.12	106 ± 19	264 ± 24	486 ± 11	12.2 ± 0.18	32.7 ± 0.4	0.66 ± 0.01
250	250	50	50	120	30	-7.52 ± 0.15	106 ± 9.1	200 ± 25	489 ± 8.2	11.1 ± 0.59	32.4 ± 0.6	0.72 ± 0.01
300	300	50	50	100	30	-8.69 ± 0.14	109 ± 14	153 ± 15	499 ± 21	10.6 ± 0.28	32.2 ± 0.9	0.75 ± 0.01
400	400	50	50	75	30	-10.5 ± 0.13	111 ± 19	130 ± 12	483 ± 8.1	9.59 ± 0.34	31.8 ± 0.7	0.81 ± 0.01
500	500	50	50	60	30	-11.7 ± 0.18	102 ± 11	116 ± 9.6	473 ± 13	9.03 ± 0.48	32.0 ± 0.6	0.85 ± 0.01
600	600	50	50	50	30	-12.7 ± 0.17	118 ± 15	107 ± 11	470 ± 7.3	8.76 ± 0.33	32.0 ± 0.9	0.87 ± 0.01
750	750	50	50	40	30	-13.8 ± 0.13	119 ± 17	99.3 ± 7.5	463 ± 15	8.48 ± 0.15	32.3 ± 0.6	0.90 ± 0.01
1000	1000	50	50	30	30	-14.9 ± 0.20	125 ± 15	92.2 ± 5.8	449 ± 8.6	7.78 ± 0.66	32.2 ± 0.6	0.93 ± 0.01
2500	2500	50	50	12	30	-17.5 ± 0.24	149 ± 14	85.1 ± 8.1	430 ± 11	6.84 ± 0.80	32.9 ± 0.6	1.01 ± 0.01
Planar	0	100	51	1	60	-22.3 ± 0.20	167 ± 16	81.3 ± 2.0	239 ± 26	6.06 ± 0.12	67.8 ± 0.6	1.14 ± 0.01

enhanced by reducing w,[23–25] leading to much improved V_{TH} and SS [Fig. 3(b)]. At w of 40 nm, the channel control is dominated by the sidewalls over the top gate, resulting in small V_{TH} of -0.08 ± 0.04 V and improved SS of 101 ± 12 mV/dec. The multi-channels are also modulated simultaneously by the tri-gate, as revealed by the g_m–V_G characteristics [Fig. 3(c)]. In transistors with planar gates or wide tri-gates ($w > 200$ nm), the g_m shows clearly five separate peaks, caused by the successive turn on of each of the five channels [inset in Fig. 3(c)]. By reducing w, these peaks merge and their full width at half maximum (FWHM) is reduced, forming finally a single sharp peak at w of 40 nm with high $g_{m,max}$ of 29.5 ± 3.6 mS/mm. This is because the V_{TH} of each parallel channel is mainly determined by the sidewall control. Thus all channels turn on simultaneously. The enhanced electrostatic control is due to the increased gate capacitance (C_G) and reduced N_s with narrowing tri-gates [Fig. 3(d)]. Such an increase in C_G does not necessarily degrade the transistor frequency performance. An optimized w of 100 nm for multi-channel tri-gate devices led to similar R_{ON}·Q_G product (15.6 ± 0.05 Ω nC) and twice the $g_{m,max}/C_G$ value (32.1 ± 0.3 MHz) as compared with planar-gate devices (16.2 ± 1.77 Ω nC and 16.1 ± 0.04 MHz), suggesting an enhanced frequency performance [Fig. 3(e)].

While tri-gates are uniquely adapted to control the multi-channels, the multi-channel structure is exceptionally suited to address the degraded $I_{D,max}$ caused by the tri-gate. As shown in Fig. 4(a), $I_{D,max}$ was greatly reduced by 17% in single-channel devices even at a large w of 1 μm, and such reduction further increased to 41% as w was reduced to 100 nm. In contrast, the $I_{D,max}$ in multi-channel devices reduced only by 6% at w of 1 μm, and remained constant until w of 150 nm. At w of 100 nm, the reduction in the $I_{D,max}$ in multi-channel devices was as small as 12%, much smaller than that in single-channel devices. This is because the multi-channel structure mitigates greatly the electron-electron and sidewall scatterings in tri-gate (MOS)HEMTs. In single-channel devices, electrons populate only one channel, resulting in a high electron density. In addition to a more pronounced electron-electron scattering, this reduces the effective distance between electrons and sidewalls, causing more sidewall scattering. Hence, $I_{D,max}$ degrades rapidly with narrower fins. The multi-channel structure addresses this issue by better distributing electrons in multiple parallel channels, instead of only one, reducing the carrier density per channel and the effective distance between electrons and sidewalls, and thus mitigating the degradation and width-dependence of $I_{D,max}$. This explanation is further supported by the dependence of $I_{D,max}$ on l [Fig. 4(b)]. Single-channel devices presented much larger and quicker degradation in

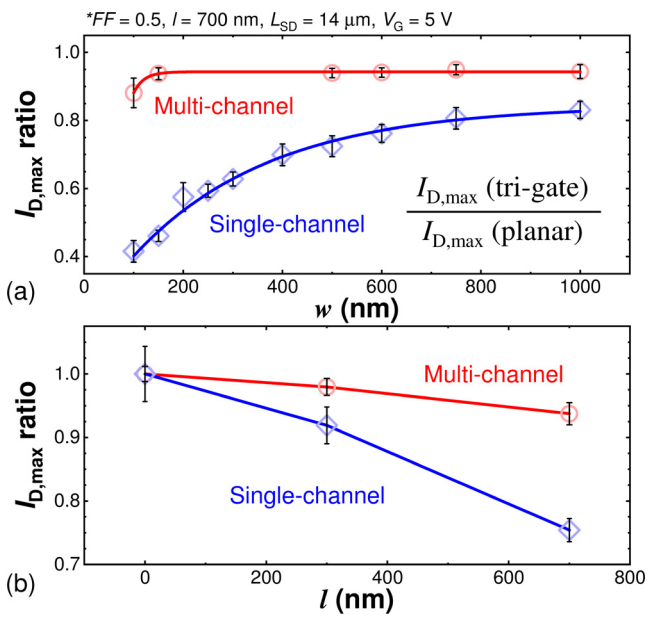

FIG. 4. Dependence of $I_{D,max}$ on (a) w and (b) l in single- and multi-channel tri-gate MOSHEMTs, all measured at $V_G = 5$ V and normalized by the width of device footprint. These devices had different w in their tri-gate regions, while sharing the same FF of 0.5 and l of 700 nm. The single-channel devices in (b) had FF of 0.64. The distance between source and drain electrodes (L_{SD}) was 14 μm.

$I_{D,max}$ as l was increased, than in multi-channel devices, indicating the higher electron velocity in multi-channel devices due to the reduced scattering.

Based on these optimizations, we designed multi-channel tri-gate GaN MOSHEMTs for high voltage applications. The L_{GD} was 10 μm to sustain high voltages, and l was 700 nm to decrease the area of etched regions on the 2DEG and reduce R_{ON}. The fins were 100 nm-wide, along with s of 100 nm and FF of 50%. The gate metal was 2.5 μm long, covering all the fins, and extended 0.5 μm and 1.3 μm towards the source and drain electrodes, respectively. Single-channel planar-gate and tri-gate GaN MOSHEMTs with similar dimensions were taken as the reference, based on a 20 nm-thick $Al_{0.25}GaN$ barrier layer, which is a typical structure used for GaN power transistors.

The multi-channel tri-gate transistors presented significantly enhanced performance as compared with conventional single-channel tri-gate transistors. As shown in Fig. 5(a), the multi-channel tri-gate architecture reduced the R_{ON} from 11.2 Ω·mm to 6.0 Ω·mm, and greatly increased the $I_{D,max}$ by more than 3.1-fold, from 252 mA/mm to 797 mA/mm [all these measurements for both kinds of devices were normalized by the width of device footprint (60 μm)]. These results are remarkable since they indicate that the multi-channel tri-gate technology can lower the conduction losses of the transistor for a given device footprint, or equivalently, deliver a given current rating in a smaller device footprint, both of which are highly beneficial for efficient power transistors.

In addition, the multi-channel tri-gate architecture also addresses the degradation in ON-state performance in single-channel tri-gate transistors [Fig. 5(a)], such as the large R_{ON} and significantly diminished $I_{D,max}$ as compared to planar-gate transistors, which is mainly due to narrower effective channels, strain relaxation, and additional spreading resistance.[26–28] The multi-channel tri-gate architecture overcomes these issues thanks to the highly conductive parallel multi-channels with fewer carriers per channel. Compared with single-channel planar-gate transistors, R_{ON} was reduced by 38% and $I_{D,max}$ was increased by 41% in the multi-channel tri-gate transistor, despite the 50% reduction in the effective channel width ($FF = 50\%$).

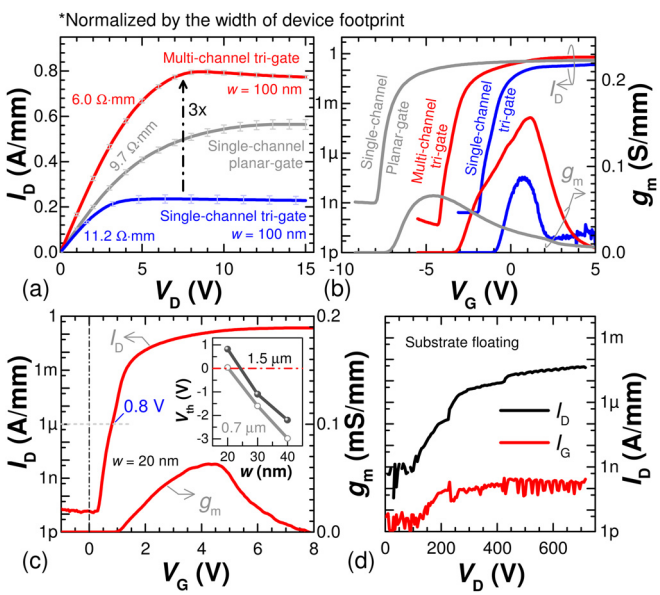

FIG. 5. (a) Output characteristics at $V_G = 5$ V and (b) transfer characteristics at $V_D = 5$ V of the transistors, normalized by the width of device footprint. The w and FF in single-channel tri-gate and multi-channel tri-gate transistors were 100 nm and 50%, respectively. (c) Transfer characteristics of multi-channel tri-gate transistors with w of 20 nm and FF of 10% at $V_D = 5$ V. (d) Typical OFF-state breakdown characteristics of the multi-channel tri-gate transistors measured with floating substrate. The inset in (c) shows the dependence of V_{TH} (at 1 μA/mm) in multi-channel tri-gate transistors on w and l.

The multi-channel tri-gate improves not only the output characteristics but also the transfer characteristics of the devices [Fig. 5(b)]. Compared to single-channel planar-gate devices, the V_{TH} in the multi-channel tri-gate transistor was reduced from −7.6 V to −3.6 V, and $g_{m,max}$ was enhanced by 2.4-fold, from 66.1 mS/mm to 156.6 mS/mm in the multi-channel tri-gate devices. The ON-state drain current (I_{ON}) was increased and the OFF-state (I_{OFF}) was diminished, resulting in a higher on/off ratio over 10^{10}.

The multi-channel tri-gate architecture also provides a promising platform to achieve normally-off operation [Fig. 5(c)]. While typical methods developed for normally-off single-channel GaN transistors such as gate recess[29] or p-GaN[30] may not deplete all embedded channels, the tri-gate offers a unique opportunity to use the sidewall-depletion effect[31] to deplete the multi-channels and achieve normally-off operation. The sidewall-depletion effect originates from surfaces states at fin sidewalls, the large work function of the gate metals, and the elastic deformation of the fins that causes more strain relaxation in the AlGaN/GaN heterostructure near the sidewalls, depleting the 2DEG in a certain width from the two sidewalls towards the center of the fin. When w is equal to or smaller than the (w_{dep}), 2DEG in the multi-channel fins will be depleted and normally-off operation can thus be achieved. As shown in Fig. 5(c), by reducing w to 20 nm ($s = 180$ nm), the 2DEG in the multi-channel fins was depleted and a positive V_{TH} of 0.82 V at 1 μA/mm was, along with I_{OFF} of only 12 pA/mm at $V_G = 0$ V, indicating excellent normally-off behavior. In addition, in this work we found that the w_{dep} was 20 nm and 24 nm for l of 700 nm and 1.5 μm, respectively [inset in Fig. 5(c)], which agrees well with other reports in the literature.[32] The larger w_{dep} for l of 1.5 μm is likely due to the greater strain relaxation within longer fins.

Despite the 3D nature of tri-gates, which leads to an increased surface area compared to conventional planar gates, the multi-channel tri-gate transistors showed very small gate leakage current of only about 0.2 nA/mm even at a high drain bias of 700 V when the transistors were in OFF state [Fig. 5(d)]. The devices presented a high hard breakdown (V_{BR}) of 715 V, indicating the potential of the proposed technology for high-voltage applications.

In conclusion, we demonstrated high-voltage multi-channel tri-gate GaN MOSHEMTs in this work, based on a unique combination of multi-channel AlGaN/GaN heterostructures and tri-gate electrodes. A significant reduction in R_{ON} and enhancement of $g_{m,max}$ were demonstrated in normally-on devices. Normally-off operation was also achieved by sidewall-depletion effect, presenting a positive V_{TH} of 0.82 V at 1 μA/mm and a high V_{BR} of 715 V. These results unveil a promising pathway for future efficient GaN power transistors with much reduced R_{ON}.

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